**MASTER SLAVE DELAY FLIP FLOP**

***MINIOR PROJECT REPORT***

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(ACCREDITED BY **NAAC** WITH **‘A’** GRADE)

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**CERTIFICATE**

This is to certify that the minor project report entitled **MASTER SLAVE DELAY FLIP FLOP** that is being submitted by **Srihari, Sai Kishore,** **Karthik** bearing **Regd. No. 171FA05078,171FA05305, 171FA05329** in partial fulfilment for the award of II year I semester B.Tech degree in Electronics and Communication Engineering to Vignan’s Foundation for Science Technology and Research, is a record of work carried out by him/her under the guidance of Ch. Suresh of ECE Department.

Signature of the faculty guide Signature of Head of the Department

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**Abstract:**

Low-power and high-speed design has become more and more important in modern VLSI circuits. The global performance of the systems is always determined by timing elements such as flip-flops and latches, thus the improvement of flip-flops is one of the most critical tasks to enhance the system performance.

The purpose of the Master-Slave is to make it edge triggered and overcome the Race-around condition and to obtain the stability in the output by inverting the clock and fed to the slave flip flop. Here we use NAND gates because it has high switching action.

**INTRODUCTION**

**Introduction of Flip-flops:**

Flip-flop is a basic memory element in digital computer. It is used to store one bit of information with 0 or 1. It is a sequential circuit. Here present state output acts as next state input. Flip flop continuously checks its inputs and changes its output correspondingly based on clock pulse. Flipflop is nothing but latch with clock pulse. Flip flop is controlled by clock pulse. Clock pulse has on period equal to off period. Flip flop is based on edge triggering of clock pulse. It may be positive edge triggered or rising edge triggered and negative edge triggered or falling edge triggered.

Flip flops are

* S R flip flop (Set –Reset)
* D flip flop (Delay or Data)
* JK flip flop (Jack Kilby)
* T flip flop (Toggle)
* Master slave flip flop

**Introduction of Master Slave D Flip Flop:**

This circuit is a [master-slave D flip-flop](http://en.wikipedia.org/wiki/Flip-flop_(electronics)#Master-slave_D_flip-flop). A D flip flop takes only a single input, the D (data) input. The master-slave configuration has the advantage of being edge-triggered, making it easier to use in larger circuits, since the inputs to a flip-flop often depend on the state of its output. The circuit consists of two D flip-flops connected together. When the clock is high, the D input is stored in the first latch, but the second latch cannot change state. When the clock is low, the first latch's output is stored in the second latch, but the first latch cannot change state.

**The Master Slave D Flip Flop:**

* The Master-Slave Flip-Flop is basically two gated SR flip-flops connected together in a series configuration with the slave having an inverted clock pulse.
* The D Flip Flop is by far the most important of the clocked flip-flops as it ensures that ensures that inputs S and R are never equal to one at the same time. The D-type flip flops are constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (Data) input.
* Then this single data input, labeled “D” and is used in place of the “Set” signal, and the inverter is used to generate the complementary “Reset” input thereby making a level-sensitive D-type flip-flop from a level-sensitive SR-latch as now S = D and R = not D.

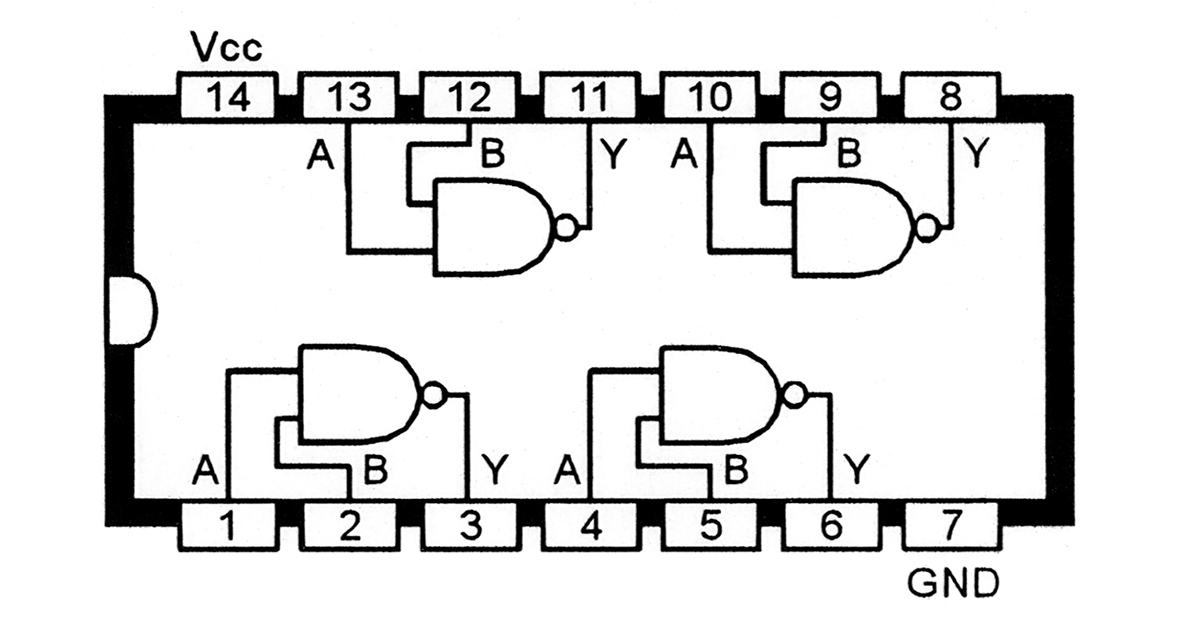
**Components Required:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **Components** | **IC Number** | **Quantity** |
| 1 | Breadboard | - | 1 |
| 2 | Two input NAND gate | IC7400 | 2 |
| 3 | NOT gate | IC7404 | 1 |
| 4 | Connecting wires | - | As required |

**Gate Description:**

**IC7400 (Two input NAND gate):**

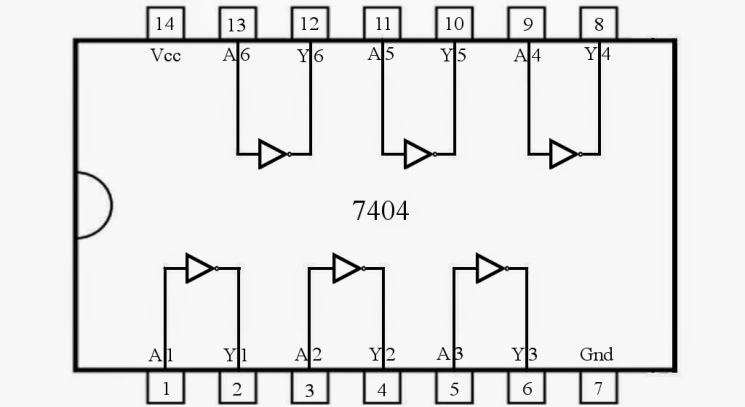
A NAND gate (NOT-AND) is a logic gate which produces an output which is false only if all its inputs are true; thus its output is complement to that of an AND gate. A LOW (0) output results only if all the inputs to the gate are HIGH (1); if any input is LOW (0), a HIGH (1) output results. A NAND gate is made using transistors and junction diodes. By De Morgan's theorem, a two-input NAND gate's logic may be expressed as AB=A+B, making a NAND gate equivalent to inverters followed by an OR gate**.**

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IC 7400 PIN Configuration

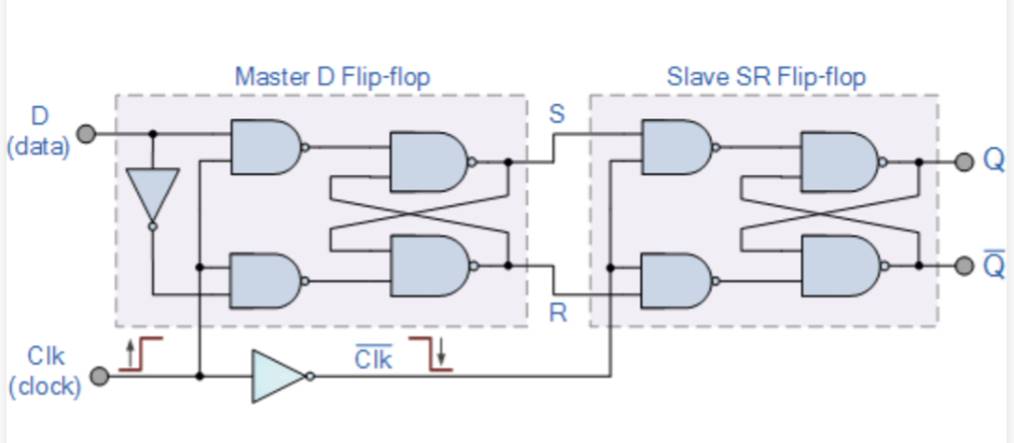
**IC7404 (NOT gate)**

A NOT gate, often called an inverter, is a nice digital logic gate to start with because it has only a single input with simple behaviour. A NOT gate performs logical negation on its input. In other words, if the input is true, then the output will be false. Similarly, a false input results in a true output

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IC 7404 PIN Configuration

**Circuit Diagram**

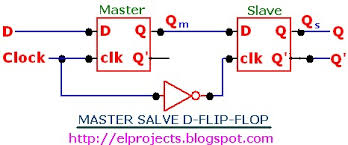
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Master Slave D flipflop

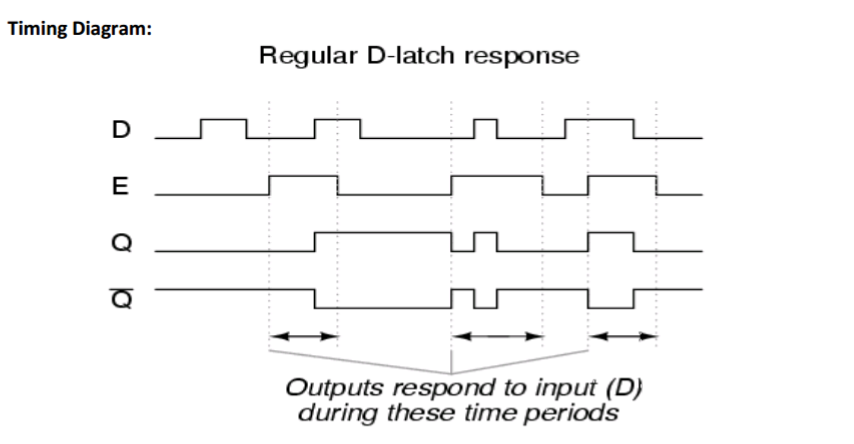
**Truth Table**

|  |  |
| --- | --- |
| INPUT | OUTPUT |

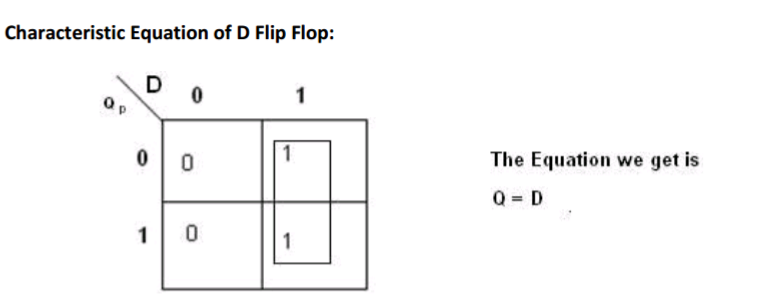
|  |  |  |  |
| --- | --- | --- | --- |
| clock | D | Q | Q’ |
| ↓ » 0 | 0 | 0 | 1 |
| ↑ » 1 | 0 | 0 | 1 |
| ↓ » 0 | 1 | 0 | 1 |
| ↑ » 1 | 1 | 1 | 0 |



Logic symbol of Master Slave D flip flop

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Timing Diagram

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Characteristic Equation of D Flip Flop

**Working of Master Slave D Flip Flop**

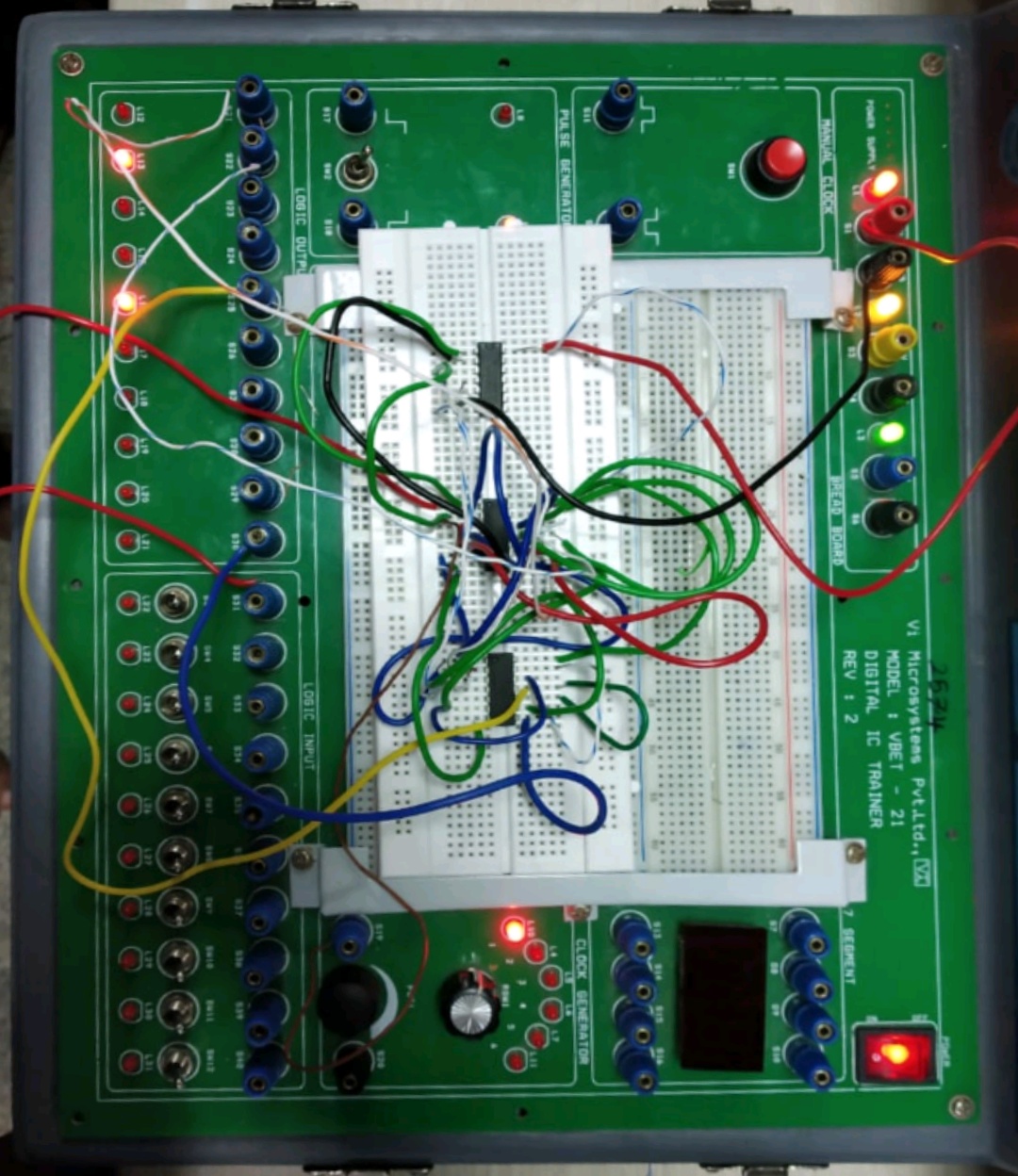
* The basic D-type flip flop can be improved further by adding a second SR flip-flop to its output that is activated on the complementary clock signal to produce a “Master-Slave D-type flip flop”.
* On the leading edge of the clock signal (LOW-to-HIGH) the first stage, the “master” latches the input condition at D, while the output stage is deactivated.
* The circuit consists of two D flip-flops connected together. When the clock is high, the D input is stored in the first latch, but the second latch cannot change state.
* When the clock is low, the first latch's output is stored in the second latch, but the first latch cannot change state.
* The result is that output can only change state when the clock makes a transition from high to low.
* On the trailing edge of the clock signal (HIGH-to-LOW) the second “slave” stage is now activated, latching on to the output from the first master circuit.
* Then the output stage appears to be triggered on the negative edge of the clock pulse. “Master-Slave D-type flip flops” can be constructed by the cascading together of two latches with opposite clock phases as shown.

**Procedure**

* Consider NOT IC as IC-1, 2 NAND ICs as IC2 and IC3.
* Every 7th pin and 14th pin of all ICs are grounded and connected to VCC.
* 1st pin in IC1 and 1st pin in IC2 are shorted and taken as input D.3rd pin of IC1 is connected to clock which is taken as input.
* Clock is connected to 2nd and 4th pin of IC2 as an input.
* 2nd pin of IC1 is connected to 5th pin of the IC2.
* 3rdand 6th pins of IC2 is connected to 9th pin and 12th pin respectively.10th pin and 11th pin are shorted.8th pin and 13th pin are shorted.
* Now, 8th and 11th pins of IC2 are connected to 1st and 5th pin of IC2 respectively.
* 4th pin of IC1 is connected to both 2nd and 4th pin of IC3. 3rd pin and 6th pin of IC3 is connected to 12th and 10th pin of IC3 respectively.
* 13th pin and 8th pin are shorted, 11th and 9th pin gets shorted.
* The final outputs are taken from 11th and 8th pin and take it as Q and Q’ respectively.

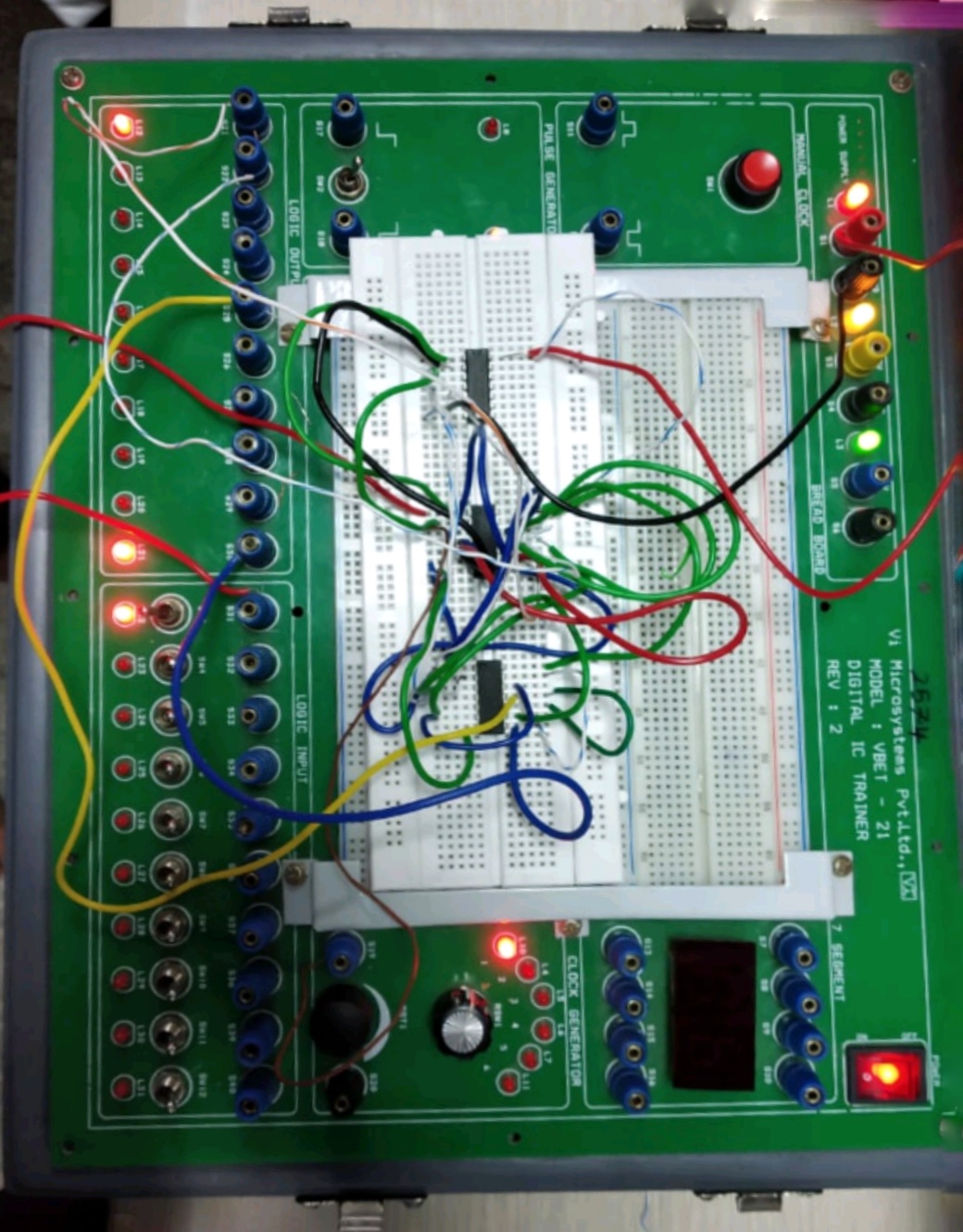
**HARDWARE OUTPUT:**

When clock is 1 and D is 0



Output picture

When clock is 1 and D is 1



Output picture

**Applications**

* Bounce elimination switch
* Data storage
* Data transfer
* Latch
* Registers
* Counters
* Frequency division
* Memory

**Conclusion**

With help of circuit diagram, we connect the IC’s on the digital IC trainer kit by means of connecting wires. Here we applied a single input to the flip flop circuit by means of not gate the applied input enters into the second nand gate. The outputs of master circuit are connected to slave inputs and the clock is also connected by using a not gate. When we triggered the clock pulse firstly, the master circuit is enabled at the same time the slave circuit is in sleep. When we change the trigger the not gate inverts the clock and now the slave circuit is enabled. At this time the master is in sleep. Finally, we designed the circuit and its truth table verified

**References**

* Rein, H.M. and Reimann, R., 1986. 3.8 Gbit/s bipolar master/slave D-flip-flop IC as a basic element for high-speed optical communication systems. *Electronics Letters*, *22*(10), pp.543-544.
* Stojanovic, V. and Oklobdzija, V.G., 1999. Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems. *IEEE Journal of solid-state circuits*, *34*(4), pp.536-548.
* Maini, A.K., 2007. *Digital electronics: principles, devices and applications*. John Wiley & Sons.